WHAT IS CLAIMED IS:

1. A method for generating at least one instruction for execution by a central processing unit, the method comprising the steps of:

receiving a misaligned instruction address;

causing an exception in response to said misaligned instruction address; and

executing, in response to said exception, an exception handling routine, said routine generating at least one instruction for execution by the central processing unit.

2. The method of claim 1, wherein said executing step comprises:

transforming data into at least one instruction;

storing said at least one instruction into memory at a first address;

loading said first address into a program counter register of said central processing unit; and

returning from execution of said exception handling routine to execute the at least one instruction stored at said first address of memory.

3. The method of claim 1, wherein said receiving step comprises the steps of:

coding a misaligned instruction address into a processor instruction;

executing said processor instruction; and

receiving a misaligned instruction address in said processor.

4. The method of claim 2, wherein said executing step further comprises a step prior to said returning step of:

performing the operations necessary to clear the exception flag and put said central processing unit into its previous execution mode.

5. The method of claim 2, wherein said executing step further comprises a step prior to said transforming data step of:

transforming said misaligned instruction address into an address where data is stored.

6. The method of claim 2, wherein said transforming data step is selected from the group consisting of: decompressing a compressed instruction, decrypting an encrypted instruction, decoding a macro instruction; transforming a non-native instruction into said at least one instruction and causing a random number of processor instruction to be performed.

7. The method of claim 5, wherein said transforming said misaligned instruction address step is selected from the group consisting of: using the misaligned instruction address, adding an offset to the misaligned instruction address and using a lookup table.

8. A computer readable medium having digital information stored thereon, the digital information defining executable computer program logic, wherein the executable computer program logic when executed performs the following steps:

receives a misaligned instruction address;

generates an exception; and

executes an exception handling routine to generate a valid instruction based on said misaligned instruction address.

9. The computer readable medium of claim 8, wherein said executing step comprises:

transforming data into at least one instruction;

storing said at least one instruction into memory at a first address;

loading said first address into a program counter register of said central processing unit; and

returning from execution of said exception handling routine to execute the at least one instruction stored at said first address of memory.

10. The computer readable medium of claim 8, wherein said receiving step comprises the steps of:

coding a misaligned instruction address into a processor instruction;

executing said processor instruction; and

receiving a misaligned instruction address in said processor.

11. The computer readable medium of claim 9, wherein said executing step further comprises a step prior to said returning step of:

performing the operations necessary to clear the exception flag and put said central processing unit into its previous execution mode.

12. The computer readable medium of claim 9, wherein said executing step further comprises a step prior to said transforming data step of:

transforming said misaligned instruction address into an address where data is stored.

13. The computer readable medium of claim 9, wherein said transforming data step is selected from the group consisting of: decompressing a compressed instruction, decrypting an encrypted instruction, decoding a macro instruction; transforming a non-native instruction into said at least one instruction and causing a random number of processor instructions to be executed.

14. The computer readable medium of claim 12, wherein said transforming said misaligned instruction address step is selected from the group consisting of: using the misaligned instruction address, adding an offset to the misaligned instruction address, and using a lookup table.

15. An apparatus for generating valid processor instructions, comprising:

first means for receiving a misaligned instruction address;

second means for generating an exception in response to said misaligned instruction address; and

third means for generating, in response to said exception, a valid instruction based on said misaligned instruction address.

16. The apparatus of claim 15, wherein said third means comprises:

means for transforming data into at least one instruction, storing said at least one instruction into memory at a first address, loading said first address into a program counter register of said central processing unit and returning from execution of said exception handling routine to execute the at least one instruction stored at said first address of memory.

17. The apparatus of claim 15, wherein said first means comprises:

means for coding a misaligned instruction address into a processor instruction, executing said processor instruction and receiving a misaligned instruction address in said processor.

18. The apparatus of claim 15, wherein said third means comprises:

means for transforming said misaligned instruction address into said valid instruction in response to said exception.

19. The apparatus of claim 15, where said third means comprises:

means for transforming said misaligned instruction into a memory address and for using said memory address to fetch said valid instruction from memory.

20. A computer system, comprising:

a processor;

a memory, coupled to said processor;

sequences of instructions, stored in said memory, which when executed by said processor define:

means for receiving a misaligned instruction address;

means for causing said misaligned instruction address to generate an exception; and

means for executing an exception handling routine in response to said exception to transform data stored in said memory into valid processor instructions.